

Notice of Allowability

Application No.

09/936,487

Applicant(s)

BARTHEL, DOMINIQUE

Examiner

Dipakkumar Gandhi

Art Unit

2133

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 9/27/2004.
2. ☒ The allowed claim(s) is/are 1-15 and 22-27, which are renumbered as 1-21.
3. ☒ The drawings filed on 25 January 2002 are accepted by the Examiner.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☒ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☒ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
 6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
 - (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
- Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08),
Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413),
Paper No./Mail Date 11/22/04
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____

A. Decary
REGISTERED PATENT EXAMINER
11/22/04

Response to Amendment

1. Amendment filed on 9/27/2004 has been entered.
2. The Examiner has withdrawn the objection to the priority claimed for the foreign application and the PCT application. It was found that the applicant had originally filed the international application on 9/10/2001. But the oath or declaration was filed later, so the filing date of 1/25/2002 was given when the 35 U.S.C. 371 requirements were met.
3. The abstract of the disclosure received with the amendment on 9/27/2004 is accepted.
4. The claims 16-21 are cancelled.

EXAMINER'S AMENDMENT

5. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with the applicant's attorney Eric S. Hyman on 11/22/2004.

The application (amendment received on 9/27/2004) has been amended as follows:

- In the amended claim 3, line 2, (ISO) should be deleted.
- In the amended claim 14,
 - Line 2, input channel (Si), clock channel (CM) is incorrect. It should be --input channel (SI), clock channel (CK).
 - Line 4-5, input channel (ST), clock channel (CM) is incorrect. It should be --input channel (SI), clock channel (CK).
- In the new claim 25, line 1, Tester according to claims 22 to 24 is incorrect. It should be -- Tester according to any one of claims 22 to 24--.

Allowable Subject Matter

6. Claims 1-15 and 22-27 are allowed.
7. The following is an examiner's statement of reasons for allowance:

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- The present invention relates to a process and a device for testing an integrated circuit comprising memory points and a Boundary Scan chain. The claimed invention (claim 1) recited features as: "Process for testing an integrated circuit comprising memory points and a Boundary Scan chain, in which one writes and/or reads to and/or from the memory points by way of an access path to the memory points from an outside terminal of the circuit, comprising: activating the Boundary Scan chain so as to impose and/or observe logic levels on the inputs/outputs of the integrated circuit."

The prior arts of record teach a built-in test architecture for testing one or more integrated circuits. Each circuit is provided with an interface compatible with IEEE standard 1149.1 and one or more scan registers containing scan cells for supplying input test data to, and receiving output test data from, the internal circuitry of the integrated circuits, a pseudo-random pattern generator for supplying patterns of test data to the boundary scan register, and a pattern compressor for compressing the output test data into a signature (Attaway et al. US 5,701,308 is an example Of such prior arts). The prior arts, however, do not teach a process for testing an integrated circuit comprising memory points and a Boundary Scan chain, in which one writes and/or reads to and/or from the memory points by way of an access path to the memory points from an outside terminal of the circuit, comprising: activating the Boundary Scan chain so as to impose and/or observe logic levels on the inputs/outputs of the integrated circuit. Hence the prior arts or record do not anticipate nor render obvious the claimed invention. Thus, claim 1 is allowable over the prior arts of record. Claims 2-11 are dependent of claim 1. Hence, claims 2-11 are also allowable over the prior arts of record.

- The claims 12-15 are allowable over the prior arts of record (see examiner's statement of reasons in the office action of 6/17/2004).
- The claimed invention (claim 22) recited features as: "Integrated circuit tester, comprising: a first module means for imposing and/or reading states of memory points of an integrated circuit, a second module means for imposing states and/or reading states of input/output cells by way of the Boundary Scan chain of the circuit simultaneously with the action of the first module."

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The prior arts of record teach a built-in test architecture for testing one or more integrated circuits. Each circuit is provided with an interface compatible with IEEE standard 1149.1 and one or more scan registers containing scan cells for supplying input test data to, and receiving output test data from, the internal circuitry of the integrated circuits, a pseudo-random pattern generator for supplying patterns of test data to the boundary scan register, and a pattern compressor for compressing the output test data into a signature (Attaway et al. US 5,701,308 is an example Of such prior arts). The prior arts, however, do not teach Integrated circuit tester, comprising: a first module means for imposing and/or reading states of memory points of an integrated circuit, a second module means for imposing states and/or reading states of input/output cells by way of the Boundary Scan chain of the circuit simultaneously with the action of the first module. Thus claim 22 is allowable over the prior arts of record. Claims 23-27 are dependent of claim 22.

Hence, claims 23-27 are also allowable over the prior arts of record.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

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Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dipakkumar Gandhi whose telephone number is 571-272-3822. The examiner can normally be reached on 8:30 AM - 5:00 PM.

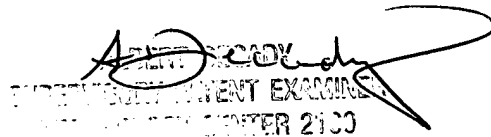
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Dipakkumar Gandhi

Patent Examiner



ALBERT DECADY
PATENT EXAMINER
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